SEMICONDUCTORS & PHOTONICS
RADIATIVE COOLING

University of Arizona researchers develop radiative cooling as a passive and energy-efficient methods that can reduce temperature-induced performance degradation and mitigate localized hotspots in semiconductor chips and other high-density integrated circuits., particularly critical with the advent of 3D-integrated CMOS technologies.

Radiative cooling is the process by which heat is dissipated by emitting thermal radiation into the cold outer space through Earth's transparent atmospheric window (8–13 µm wavelength). Mohamed ElKabbash and his team focused on improving radiative cooling efficiency by developing angular-selective emitters that minimize absorption of environmental radiation, thus maintaining effective cooling under humid and other challenging conditions.

Radiative cooling of electronics

Expanding the application of radiative cooling, the team demonstrated strategies to significantly enhance the efficiency of thermoelectric generators (TEGs). Specifically, they transformed the cold side of TEGs into optimized thermal emitters via femtosecond laser processing and anodization of aluminum surfaces to form structured aluminum oxide matrices with superior radiative cooling characteristics. This approach markedly increased the temperature gradient across TEGs, improving their overall energy conversion efficiency.

Designs meet established semiconductor fabrication processes

The team also created a CMOS metal optics platform that enables the integration of optical functionalities directly into standard CMOS manufacturing processes. By repurposing existing back-end-of-the-line (BEOL) metal interconnect layers in CMOS chips, the researchers designed nanoscale metallic structures that can control light at optical frequencies using standard CMOS foundry processes. This platform allows conventional metal wiring structures within CMOS chips to function not just as electrical interconnects but also as efficient optical components.

The team is investigating designs where metal interconnects in the CMOS BEOL serve as directional thermal emitters (**Figure 1**). These designs adhere to existing foundry design rules to ensure direct implementation into established semiconductor fabrication processes without requiring additional manufacturing steps.

Hotspot mitigation for next-generation microelectronics

3D stacking of integrated circuits (ICs) concentrates power in small regions and introduces thermal barriers, leading to thermal power concentration and steep temperature gradients that are difficult to cool. We engineer nanowires to act as resonant infrared (thermal) antennas due to their large effective areas compared to their physical dimensions. Our radiative cooling approach that embeds these wires in the BEOL to dissipate heat promises an increase in the total power removed from the chip by up to 20% (**Figure 2**). This extra cooling channel is especially useful in areas where thermal isolation limits the overall conduction efficiency.

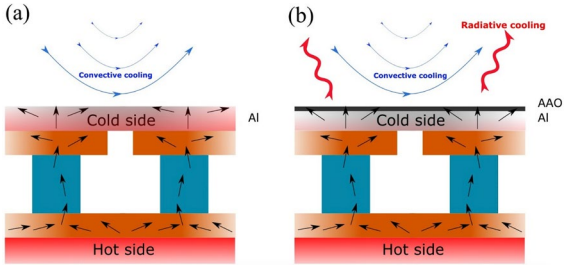

Figure 1: Schematics of enhanced thermoelectric generation through radiative cooling. The cold side of the thermal generator has near unity thermal emissivity.

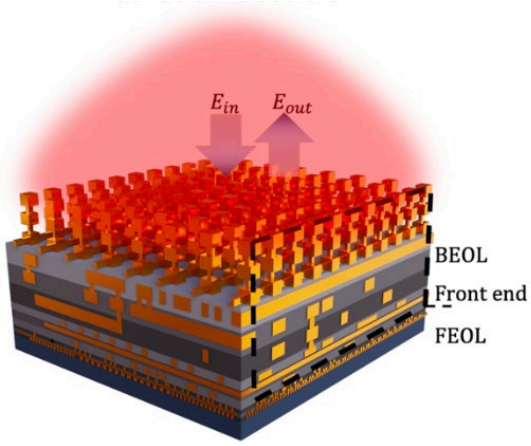

Figure 2: Nanoengineered thermally-emitting wires as radiative coolers. Wires are integrated within the BEOL of CMOS chips for passive radiative cooling. Engineered metal interconnects serve as directional thermal emitters, dissipating excess heat as infrared radiation into a heat sink while adhering to standard foundry design rules.

Mohamed ElKabbash, PhD | Assistant Professor
Optical Sciences | melkabbash@arizona.edu

Mohamed is an assistant professor in the Wyant College of Optical Sciences. He leads the Quantum Photonics & Nanophotonics Group. He was a postdoc in MIT's Quantum Photonics Group. He works on quantum photonics, nanophotonics and metamaterials, and ultrafast light-matter interaction.